

TABLE 1 LOW-POWER TOOLS

Company	Tool/ starting price	Tasks	Where used in flow?	Description
Apache Design	RedHawk-LP/ \$95,000	Analysis	Postlayout (DEF/ GDS)	Low-power-design analysis and optimization tool, including rush-current and ramp-up analysis, full-chip mixed-mode verification, and switch optimization for MTCMOS designs
	RedHawk-ALP/ \$150,000	Analysis	Postlayout (DEF/ GDS)	Extends RedHawk-LP to include ultralow-leakage-design techniques, such as substrate back-biasing (VTCMOS), power-gated memories, and on-chip low-dropout voltage regulators
ArchPro Design Automation	MVSim/ NA	Analysis and verification	RTL, gate level	Cosimulator that simulates multivoltage effects with electrical accuracy; users can identify multivoltage issues using automatic assertion generation and analyze coverage of multivoltage states
	MVRC/ NA	Analysis and verification	RTL, gate level	Vectorless verification of multivoltage issues; users can detect topological, functional, and sequential issues with respect to power-management control
	MVSyn/ NA	Design	RTL, gate level	Automatic insertion of level shifters and isolation cells at RTL and gate level; users can perform electrically accurate simulations at the RTL/gate level with the inserted cells
Atrenta	Spyglass- Power/ \$60,000	Analysis	RTL, postsynthesis, after place and route	Provides a comprehensive approach to low-power design; helps manage power and voltage domains
Azuro	PowerCentric/ NA	Design and analysis	Gate level, postphysical	Operates as a complete replacement for clock-tree synthesis within digital-design flows, comprehensively addressing power, timing, and variability within one unified optimization environment
Bluespec	ESEComp/ \$25,000	Design	ESL, RTL	Synthesizes SystemC designs into highly efficient Verilog RTL; enables rapid architectural exploration; accelerates the correct implementation of multiple clock domains, clock synchronizers, and gated clocks
	BSC/ \$25,000	Design	ESL, RTL	Synthesizes Bluespec SystemVerilog designs into highly efficient Verilog Design; Bluespec's synthesis tools enable rapid architectural exploration and accelerate the correct implementation of multiple clock domains, clock synchronizers, and gated clocks
Cadence Design Systems	Cadence Low- Power Solution/ NA	Design and analysis	RTL, gate level, transistor level	Integrates logic-design, verification, and implementation technologies with the Si2 CPF; reduces risk; improves productivity; achieves superior trade-off among timing, power, and area requirements
	Encounter RTL Compiler global synthesis/ NA	Design and analysis	RTL, gate level	Performs top-down multiobjective, multidomain, multimode synthesis for exploration and synthesis of multiple threshold voltages, multiple supplies, power shutoff, and voltage scaling, using CPF to sustain design intent
	Encounter Conformal Low Power/ NA	Analysis	RTL, gate level, transistor level	Verifies and debugs power-optimized multimillion-gate designs using CPF and combining low-power structural and functional checks with equivalence checking for superior performance, capacity, and ease of use
	Encounter Test/ NA	Design	Gate level	Creates test mode for each power domain, including shut-off requirements, as specified in CPF; inserts structures to control power during test; generates ATPG vectors that reduce power consumption during test

Table continues on page 62

TABLE 1 LOW-POWER TOOLS

Company	Tool/ starting price	Tasks	Where used in flow?	Description
	SoC Encounter/ NA	Design and analysis	Gate-to-GDSII	Implements low-power designs; includes multiple-power-domain support for virtual prototyping, placement, and optimization; provides autoinsertion of low-power structures, such as switch cells and isolation cells; includes power-aware clock-tree synthesis, domain-aware routing, analysis of power consumption and IR-drop effects
	Voltagestorm/ NA	Analysis	Gate level	Integrates static- and dynamic-power-rail verification in CPF-enabled SoC Encounter; performs sign-off power analysis; automates analysis and optimization of decoupling capacitance size and location, resulting in lower dynamic-IR drop
	Incisive Design Team and Enterprise Manager/ NA	Verification	System level, RTL, gate level	Creates power plan and metrics in CPF-enabled flow; tracks power verification metrics against design and verification plan, ensuring full coverage-driven verification of all power-modes in the design
	Incisive Design Team and Enterprise Simulator/ NA	Verification	System level, RTL, gate level	Uses CPF for seamless verification of power shutoff without changing the verification environment; reduces risk of power-shutoff failure
	Incisive Formal Verifier/ NA	Verification	System level, RTL, gate level	Verifies power intent using standard assertion languages, complex power-control modules, and state and sequence relationships versus CPF specification; identifies corner cases without time-consuming simulation
	Paladium III/ NA	Verification	System level, RTL, gate level	Emulates system-level behavior, including both software and hardware, to quickly verify complex power-shutoff relationships
	Xtreme III/ NA	Verification	RTL, gate level	Reduces verification risk by seamlessly and rapidly verifying power shutoff without changing the RTL or verification environment
ChipVision Design Systems	Orinoco/ \$150,000	Design and analysis	Above RTL (system level)	Optimizes for low power at the electronic-system level to gain significant reduction of energy consumption
Golden Gate Technology	PowerGold/ \$250,000 per year list price	Power optimization	Postsynthesis physical design, gate level	Reduces power by 10 to 20% or more without impacting timing and complementing Cadence, Synopsys, or Magma flows
Magma Design Automation	Talus Power/ NA	Design	RTL-to-GDSII	Enables optimal power management throughout the flow with power-aware synthesis, physical optimization, power-aware CTS, automated multivoltage, multiple threshold voltage, and MTCMOS methodology, allowing designers to minimize power and ensure uniform power distribution
	Quartz Rail/ NA	Analysis	RTL-to-GDSII	Analyzes power-integrity sign-off for power, IR drop, and thermal effects with a built-in SPICE engine for accurate results
Mentor Graphics	Questa 6.3/ TBD	Analysis	RTL, gate level	Simulates power shutdown and power-up of power domains; provides voltage scaling to reduce power gating and retention behavior in designs
	0-In CDC/ TBD	Analysis	RTL	Uses clock gating to reduce dynamic-power consumption; ensures the design has no clock-domain-crossing issues
Sequence Design	PowerTheater/ \$115,000	Design and analysis	RTL, gate level	Provides RTL power analysis and management with silicon-aware features for voltage islands, multiple threshold voltages, power gating, and clock gating

Table continues on page 64

TABLE 1 LOW-POWER TOOLS

Company	Tool/ starting price	Tasks	Where used in flow?	Description
	CoolTime/ \$130,000	Analysis	Physical design	Provides dynamic voltage-drop analysis and optimization; analyzes timing, signal integrity, static-IR drop, and electromigration; supports design techniques, such as voltage islands, multiple threshold voltages, power gating, and clock gating
	CoolCheck/ \$80,000	Analysis	Physical design	Provides early power-grid debugging with a fast formal technique for finding missing vias, weak connections, and highly resistive current paths in the power grid
	CoolPower/ \$240,000	Design and analysis	Postroute design closure	Provides automatic, concurrent optimization of leakage power, dynamic power, timing, and signal integrity, including multiple threshold voltages and MTCMOS power-gating optimizations
Synopsys	VCS/ \$36,750	Verification	RTL, gate level	Provides comprehensive functional verification with built-in testbench, coverage, assertion, and debugging technology; supports power-aware verification, including correct handling of retention registers, and power-up/power-down sequences
	Leda/ \$14,945	Analysis	RTL, gate level	Provides programmable RTL design and coding-guideline checker and built-in checks for CDC, SDC, power, and test; provides more than 50 low-power checks, including insertion/location of level shifters and isolation cells and clock gating to turn off power regions
	Design Compiler Ultra/ \$98,000	Design	RTL	Provides comprehensive RTL synthesis, delivering best productivity; includes power and test-aware Topographical Technology
	Power Compiler (add- on to Design Compiler Ultra)/ \$50,470	Design	RTL, gate level	Provides complete power-management synthesis for achieving the lowest power design; supports multivoltage, MTCMOS power gating, multithreshold leakage and gate-level power optimization, clock gating, and operand isolation
	DFT MAX (add-on to DFT Compiler)/ \$123,725	Design	Gate level	Provides power-aware adaptive-scan compression for test data and time reduction
	IC Compiler/ \$757,050	Design and analysis	Gate level	Provides complete physical implementation, including hierarchical-design planning with automated power-network synthesis and analysis; provides single convergent flow from netlist to silicon with support for multivoltage designs, multithreshold leakage, low-power placement and CTS, and state-retention power gating
	PrimeTime PX/ \$24,500	Analysis	Gate level, TTL	Provides concurrent timing, signal integrity, and power analysis
	PrimeRail/ \$176,645	Analysis	Gate level, TTL	Offers power-integrity sign-off with full-chip dynamic-power-integrity tool; provides cell- and transistor-level dynamic-voltage-drop and electromigration analysis
	TetraMAX/ \$54,145	Analysis	Gate level	Offers power-aware manufacturing-test-pattern generation for designs incorporating scan design-for-test techniques, including compression
Innovator/ \$60,000	Preimplemen- tation	Transaction (system) level	Provides software-driven power analysis and optimization with power-aware system software to measure the effects of architecture, power-management techniques, and software on power dissipation	